





BSS8402DWK

COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET

Product Summary

Device	V _{(BR)DSS}	R _{DS(ON)} max	I _D max T _A = +25°C
Q1	60V	5Ω @ V _{GS} = 5V	150mA
Q2	-50V	10Ω @ V _{GS} = -5V	-100mA

Description

This MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- **Power Management Functions**
- Analog Switch



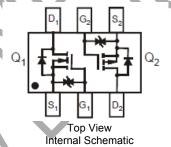


Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- **ESD Protected Gate**
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 standards for High Reliability

Mechanical Data

- Case: SOT363
- Case Material: Molded Plastic. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish annealed over Alloy 42 leadframe (Lead Free Plating). Solderable per MIL-STD-202, Method 208 @3
- Terminal Connections: See Diagram
- Weight: 0.006 grams (approximate)



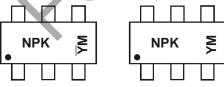
Ordering Information (Note 4)

Part Number	Compliance	Case	Packaging
BSS8402DWK-7	Standard	SOT363	3,000/Tape & Reel
BSS8402DWK-13	Standard	SOT363	10,000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green"
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site Shanghai A/T Site NPK = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test site) YM = Date Code Marking for CAT (Chengdu Assembly/ Test site)

Y or \overline{Y} = Year (ex: A = 2013)

M = Month (ex: 9 = September)

Data Coda Kay

Year	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016
Code	Р	R	S	Т	U	V	W	Х	Υ	Z	Α	В	С	D
Month	Jan	Feb	М	ar	Apr	May	Jun	Jul	Aug	Se	р	Oct	Nov	Dec
Code	1	2	3	3	4	5	6	7	8	9		0	N	D



Maximum Ratings – Total Device (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Power Dissipation (Note 5)	P _D	300	mW
Thermal Resistance, Junction to Ambient(Note 5)	R _{θJA}	423	°C/W
Power Dissipation (Note 6)	P _D	400	mW
Thermal Resistance, Junction to Ambient(Note 6)	$R_{\theta JA}$	312	°C/W
Operating and Storage Temperature Range	T _{J,} T _{STG}	-55 to +150	°C

Maximum Ratings N-CHANNEL - Q₁, 2N7002 Section (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Units
Drain-Source Voltage		V_{DSS}	60	V
Gate-Source Voltage	Continuous	V _{GSS}	±20	V
Drain Current (Note 5)	Continuous	I _D	150	mA

Maximum Ratings P-CHANNEL - Q₂, BSS84 Section (@T_A = +25°C, unless otherwise specified.)

Characterist	ic	Symbol	Value	Units
Drain-Source Voltage		V _{DSS}	-50	V
Gate-Source Voltage	Continuous	V _{GSS}	±12	V
Drain Current (Note 5)	Continuous	I _D	-100	mA

Electrical Characteristics N-CHANNEL - Q₁, 2N7002 Section (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	60	_	_	V	$V_{GS} = 0V, I_D = 10\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}			1.0	μA	$V_{DS} = 60V$, $V_{GS} = 0V$	
Gate-Body Leakage	I _{GSS}			±10	μA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	V _{GS(th)}	1.0		2.5	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	
Static Drain-Source On-Resistance	P			3	Ω	V _{GS} = 10V, I _D = 0.20A	
	R _{DS(ON)}	_	_	5	5.2	V _{GS} = 5V, I _D = 0.15A	
Forward Transconductance	g FS	80		_	mS	V _{DS} =10V, I _D = 0.2A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}		54.2		pF		
Output Capacitance	Coss	_	4.2		pF	$V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz$	
Reverse Transfer Capacitance	C _{rss}		2.7		pF		
SWITCHING CHARACTERISTICS (Note 8)							
Turn-On Delay Time	t _{D(on)}		3.3		ns		
Turn-On Rise Time	t _r	_	2.2		ns	$V_{DD} = 30V, I_D = 0.2A,$	
Turn-Off Delay Time	t _{D(off)}	_	18.5		ns	$R_L = 150\Omega$, $V_{GEN} = 10V$, $R_{GEN} = 25\Omega$	
Turn-Off Fall Time	t _f	_	2.1		ns	1	



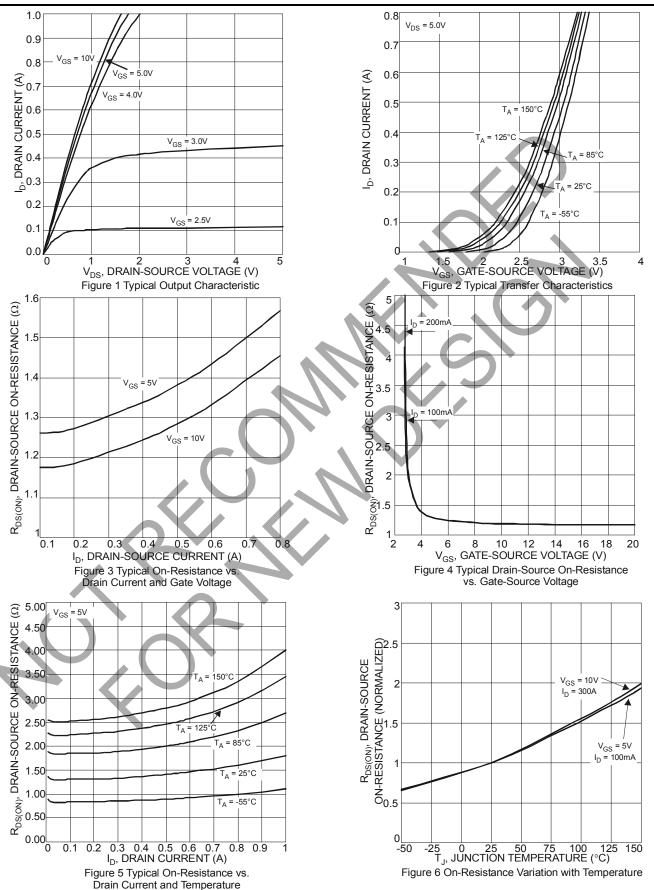
Electrical Characteristics P-CHANNEL – Q₂, BSS84 Section (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)			71			
Drain-Source Breakdown Voltage	BV _{DSS}	-50	_	_	V	V _{GS} = 0V, I _D = -250μA
Zero Gate Voltage Drain Current	I _{DSS}	_	_	-15	μA	V _{DS} = -50V, V _{GS} = 0V
Gate-Body Leakage	I _{GSS}	_	_	±10	μA	V _{GS} = ±12V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(th)}	-0.65	_	-2.0	V	$V_{DS} = V_{GS}$, $I_D = -1mA$
Static Drain-Source On-Resistance	R _{DS (on)}	_	_	10	Ω	$V_{GS} = -5V, I_D = -0.1A$
Forward Transconductance	g FS	50	_	_	mS	V _{DS} = -25V, I _D = -0.1A
DYNAMIC CHARACTERISTICS (Note 8)	•					
Input Capacitance	C _{iss}		48		pF	V
Output Capacitance	Coss	_	3.3		pF	$V_{DS} = -25V$, $V_{GS} = 0V$, $f = 1.0MHz$
Reverse Transfer Capacitance	C _{rss}	_	2.0		pF	
SWITCHING CHARACTERISTICS (Note 8)						
Turn-On Delay Time	t _{D(on)}	_	3.3	1	ns	
Turn-On Rise Time	t _r	_	2.5		ns	$V_{DD} = -30V$, $I_D = -0.27A$,
Turn-Off Delay Time	t _{D(off)}	_	42.4		ns	$R_{GEN} = 50\Omega$, $V_{GS} = -10V$
Turn-Off Fall Time	t _f	_	14.3		ns	

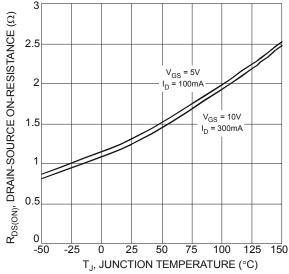
- Device mounted on FR-4 PCB, with minimum recommended pad layout
 Device mounted on 1" x 1" FR-4 PCB with high coverage 2oz. Copper, single sided.
 Short duration pulse test used to minimize self-heating effect.
 Guaranteed by design. Not subject to product testing.

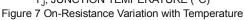


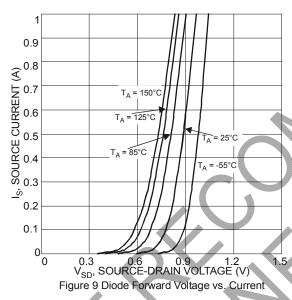
N-Channel MOSFET

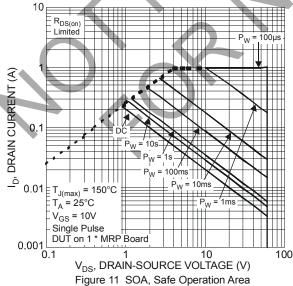












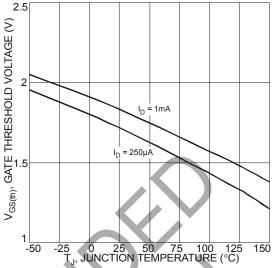
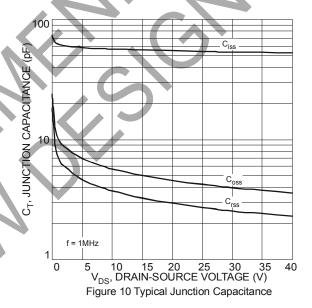
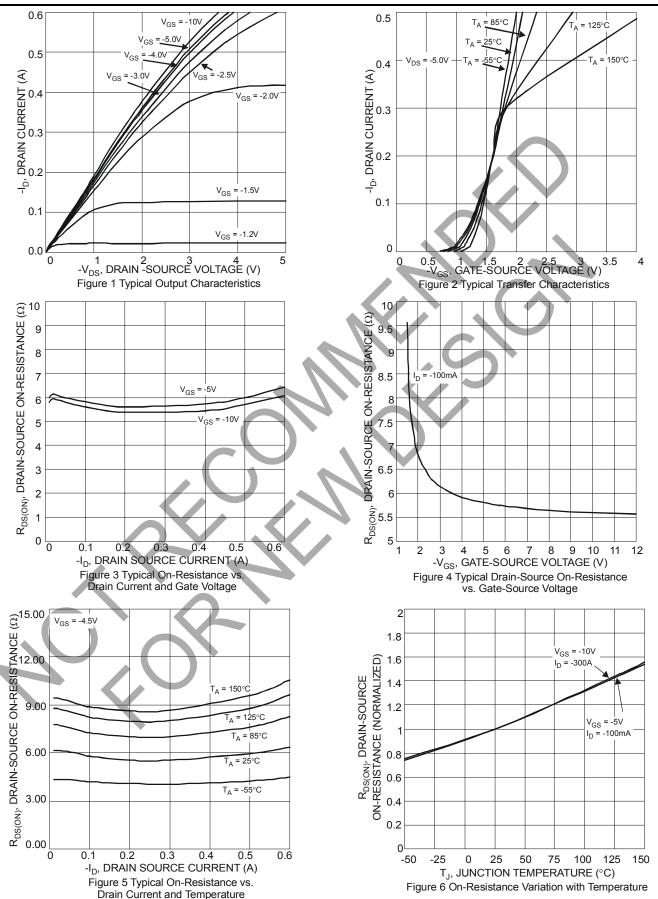


Figure 8 Gate Threshold Variation vs. Ambient Temperature

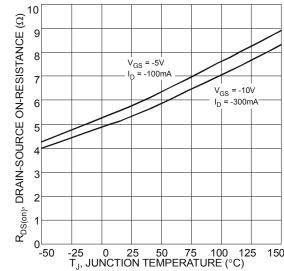




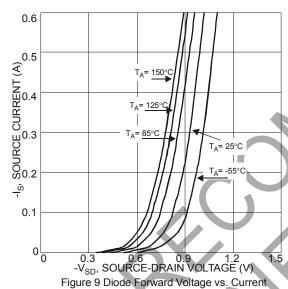
P-Channel MOSFET

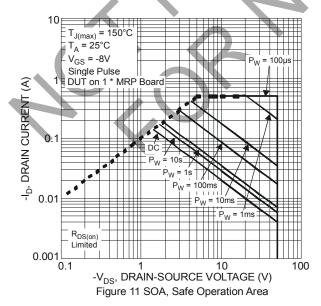












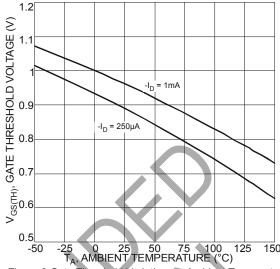
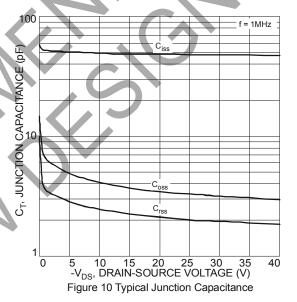


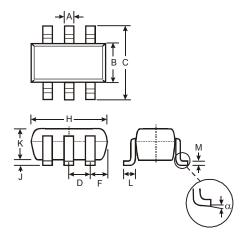
Figure 8 Gate Threshold Variation vs. Ambient Temperature





Package Outline Dimensions

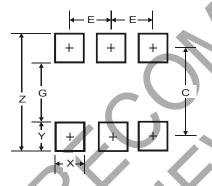
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



	SC	T363					
Dim	Min	Тур					
Α	0.10	0.30	0.25				
В	1.15	1.35	1.30				
С	2.00	2.20	2.10				
D	0.65 Typ						
F	0.40	0.45	0.425				
Н	1.80	2.20	2.15				
J	0	0.10	0.05				
K	0.90	1.00	1.00				
L	0.25	0.40	0.30				
М	0.10	0.22	0.11				
α	0°	8°					
All	All Dimensions in mm						

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.5
G	1.3
Х	0.42
Y	0.6
С	1.9
F	0.65



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